SPECIFICATION AMENDMENTS

Replace the paragraph beginning at page 1, line 16 with:

For example, if a trigger is input to the circuit of the semiconductor device by external surge or the like, a parasitic thyristor formed in the circuit of the semiconductor device is turned on, sometimes resulting in occurrence of latch-up so that excessive current continuously flows. Specifically, in a lower driving output transistor in a three-phase lower arm used in a driver inverter integrated circuit (IC) or the like for a motor, a back electromotive force is derived from motor driving coils at the time of switching the transistor, and unnecessary negative potential is produced. Thus, the latch-up poses a serious problem.

Replace the paragraph beginning at page 2, line 1 with:

If attention is paid to structure of a metal oxide semiconductor (MOS) transistor in the semiconductor device, it is found that the following parasitic transistors are formed in the MOS transistor. In an N channel MOS transistor (referred to as "NMOS" hereinafter), a parasitic NPN transistor consists of the following layers and region functioning as emitter, base, and collector, respectively. That is, the parasitic NPN transistor consists of an N well forming a drain region of NMOS, an N type buried layer formed right under the N well and on a P type silicon substrate, the P type silicon substrate, and an island region formed on an N type silicon layer that is formed at an isolated position from this NMOS, functioning as emitter, base, and collector. For example, if negative voltage is applied to the drain that functions as the emitter, the parasitic NPN transistor operates to extract current from ~~another~~ other island regions formed on an N type silicon layer. If this extracted current is large, the NPN transistor causes the semiconductor device to malfunction. Further, if the parasitic NPN transistor thus produced and a parasitic PNP transistor produced at the other location form a parasitic thyristor, the thyristor is turned on by external surge or the like to cause latch-up and the elements of the semiconductor device are thermally ~~fractured~~ destroyed at the worst.

Replace the paragraph beginning at page 6, line 15 with:

Fig. 2 schematically shows the sectional structure and circuit diagram of an NMOS transistor according to a first embodiment of the present invention;

Replace the paragraph beginning at page 6, line 18 with:

Fig. 3 schematically shows the sectional structure and circuit diagram of the NMOS transistor if an N- epitaxial region is not grounded to a ground potential; and

Replace the paragraph beginning at page 6, line 21 with:

Fig. 4 schematically shows the sectional structure and circuit diagram of an NMOS transistor according to a second embodiment of the present invention.